# Fundamental Limits on Energy Efficiency Performance of VCO-Based ADCs

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***Abstract*—In systems constrained by battery power or scavenged energy limits, ADC energy efficiency as expressed by the fJ/step figure-of-merit is a critical design driver. This paper describes a time-domain approach to determine the fundamental limit on ADC performance for techniques such as VCO-based ADCs which perform the ADC function in the time domain.**

## I. Introduction

Low-cost energy-efficient analog-to-digital converters (ADCs) are needed in many rapidly growing mixed-signal application areas. Scaling of CMOS to nanometer dimensions has enabled dramatic improvement in digital power efficiency; however, most traditionally dominant ADC architectures are not well suited to the lower supply voltage environment. The improvement in time resolution enabled by increased digital speeds naturally drives design toward time-domain ADC architectures such as voltage-controlled-oscillator (VCO) based ADCs. Recent work has improved fJ/step performance by reducing the overhead of additional circuitry required to mitigate VCO nonlinearity.

This paper investigates the fundamental limit achievable for efficiency of the VCO-based approach. First, section II describes aspects of CMOS scaling for digital applications that are relevant to performance of time-based ADC techniques. Next, section III presents a brief overview of the VCO-based approach and previous techniques to improve linearity in VCO-based ADCs. Section IV provides quantitative limits on achievable fJ/step performance for VCO based ADCs, and simulation results for a reconfigurable VCO-based ADC in a 45nm CMOS process are presented in Section V.

TABLE I
Performance for CMOS process nodes 130nm - 32nm.

| Reported | | | | Calculated | |
|---|---|---|---|---|---|
| Process node $nm$ | $V_{DD}$ | Ring oscillator frequency (31 stage) | Energy per gate transition nW / $MHz \cdot gate$ | Gate delay $t_{PD}$ [psec] | Effective total gate capacitance $C_{L(TOT)}$ [fF] |
| 130 | 1.2 | 448 MHz | 4.42 | 36.0 | 3.07 |
| 90 | 1.2 | 524 MHz | 3.04 | 30.8 | 2.11 |
| 65 | 1.2 | 695 MHz | 2.07 | 23.2 | 1.44 |
| 45 | 1.0 | 2.69 GHz | 1.51 | 6.00 | 1.51 |
| 32 | 0.9 | 3.53 GHz | 1.30 | 4.57 | 1.60 |

## II. Implications of CMOS Scaling

Table I shows performance parameters reported for process evaluation structures at a semiconductor manufacturer available through the MOSIS consortium [1], indicating the general trend of increasing speed of operation and improved logic transition power efficiency as expressed in energy required per gate transition. From the reported data, the gate propagation delay $t_{PD}$ can be calculated, as well as effective total capacitance per gate $C_{L(TOT)}$ from the total energy $C_{L(TOT)}V_{DD}^2$ per transition. Plotting these calculated results in Figure 1 shows the general trend toward reduced gate delay, with effective total capacitance approaching $\approx 1.5$fF.

The decreasing trend of supply voltage $V_{DD}$ limits signal swing, making a given SNDR goal more difficult to achieve for traditional voltage-domain ADC architectures. The improvement in time resolution enabled by shorter gate delay $t_{PD}$ naturally drives design toward time-domain ADC architectures such as VCO-based ADCs [2]–[15].

## III. VCO-Based ADC Overview

### A. Operating principle of simplified VCO-based ADC

For illustrating the fundamental operating principles of the proposed work, Figure 2 shows a simplified VCO-based ADC in conceptual form. The ADC input $v_{IN}$ is applied as the control input $v_{CTL}$ of a ring oscillator VCO. In its simplest form, the frequency-to-digital converter is essentially a phase counter: The ring phases $\phi_A, \phi_B, \phi_C$ are sampled and the number of oscillator cycles is counted. The result at the end of the conversion time is the ADC output $n$, the total number

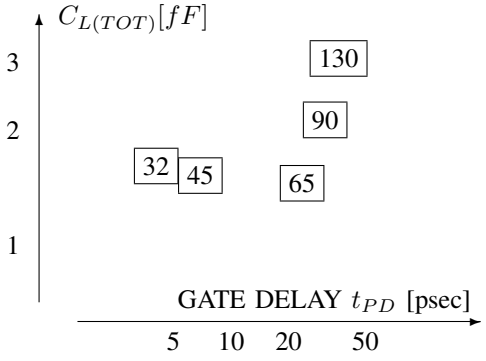


Fig. 1. CMOS scaling trend.

of phase transitions observed in the time $T_{CONV}$. From the timing diagram in Fig. 2, the output $n$ is given simply by

$$n = \frac{T_{CONV}}{t_{PD}} \tag{1}$$

in which $t_{PD}$ is the ring oscillator gate delay time. For a current-starved gate architecture, we can approximate the MOSFET drain current $i_D$ during the gate delay time $t_{PD}$ as

$$i_D = G_m v_{IN} \tag{2}$$

in which $G_m$ describes the slope of the $V_{GS} \rightarrow I_D$ relationship for the $M_{CTL}$ MOSFETs. To develop the simplified operating principle of the VCO-based ADC, we temporarily make the (admittedly unreasonable but) simplifying assumption that this relationship is linear. Techniques for mitigating the effects of nonlinearity will be described in the following subsection.

For a conservative approximation of the gate propagation delay, we apply charge conservation as the gate output drives the total load capacitance $C_L$ over a peak-to-peak voltage swing of $V_{DD}$ in time $t_{PD}$ with drain current $i_D$ as

$$i_D = \frac{C_L V_{DD}}{t_{PD}} \quad \Rightarrow \quad t_{PD} = \frac{C_L V_{DD}}{i_D} \tag{3}$$

Combining (1), (2) and (3) gives for the output $n$

$$n = \left(\frac{T_{CONV}}{C_L/G_m}\right)\frac{v_{IN}}{V_{DD}} \tag{4}$$

From (4) we see that the output $n$ is proportional to the input $v_{IN}$, which is the desired relationship for an ADC.

### B. Previous work

A major difficulty with the simplified approach of Figure 2 is that ADC linearity and SNDR depend directly on the linearity of the VCO voltage-to-frequency control characteristic, which is in general poorly controlled. In practice, VCO nonlinearity limits SNDR to no better than $\approx 40$ dB [15].

Figure 3 summarizes reported performance for previously published work, with linearization techniques including:

- Use of the VCO as an integrator in a $\Sigma - \Delta$ feedback loop, reducing effects of VCO nonlinearity [2]–[10], [14].
- Reduction of input signal amplitude to avoid nonlinear portions of the transfer characteristic [5].
- Degeneration to linearize the voltage-to-current characteristic in a current-starved VCO [12]
- Foreground calibration [6], [10], [11], [13] .

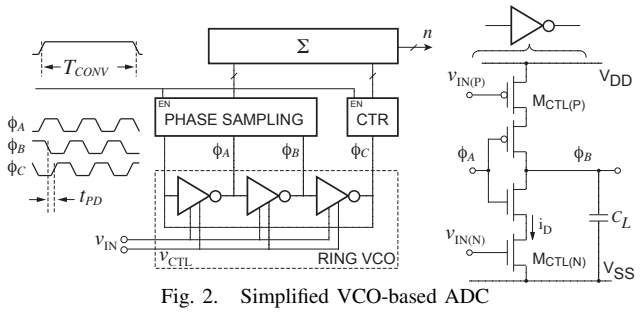


Fig. 2. Simplified VCO-based ADC

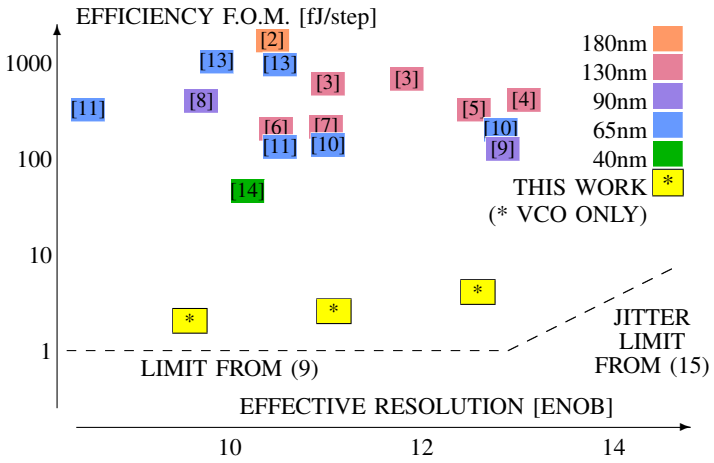


Fig. 3. Survey of VCO-based ADCs.

Another aspect of additional complexity, whether analog or digital, is the effect of the additional circuitry on ADC power consumption. Figure 3 plots the reported efficiency F.O.M. as a function of effective-number-of-bits resolution. The wide range of performance shown in Figure 3 motivates the following analysis of fundamental limits on energy efficiency.

## IV. Fundamental Limits

### A. Quantization limited

In this section we adopt the following assumptions:

1) VCO jitter is negligible over conversion time $T_{CONV}$
2) Linearity has been corrected such that ENOB is limited by unshaped quantization noise
3) Power consumption is dominated by VCO
4) Time resolution is limited by the gate delay $t_{PD}$ (no phase interpolation used)

An advantage of analyzing the simplified ADC of Figure 2 with these assumptions is that we can develop a simple expression for the fundamental limit on the efficiency figure-of-merit, defined as

$$FOM = \frac{P_{DISS}}{f_S \cdot 2^{ENOB}} \left[\frac{J}{step}\right] \tag{5}$$

To find this limit we need the power dissipation, sampling frequency, and effective resolution.

The worst-case maximum power dissipation will occur for the maximum current $i_D$, which from (3) will occur for the minimum gate delay $t_{PD(MIN)}$:

$$i_{D(MAX)} = \frac{C_L V_{DD}}{t_{PD(MIN)}} \tag{6}$$

which gives for $P_{DISS}$

$$P_{DISS} = i_{D(MAX)} V_{DD} = \frac{C_L V_{DD}^2}{t_{PD(MIN)}} \tag{7}$$

To find the limit of best achievable performance for the effective-number-of-bits expression $2^{ENOB}$, we will use the

ADC resolution $n_{MAX}$, the maximum number of counts $n$. Using $t_{PD(MIN)}$ in (1) we have

$$n_{MAX} = \frac{T_{CONV}}{t_{PD(MIN)}} \tag{8}$$

Using for the sampling frequency $f_S = 1/T_{CONV}$ in (5) with (7) and (8) gives

$$\frac{C_L {V_{DD}}^2}{t_{PD(MIN)}} T_{CONV} \frac{t_{PD(MIN)}}{T_{CONV}} \Rightarrow \boxed{FOM = C_L V_{DD}^2} \tag{9}$$

Referring to values for $C_L$ and $V_{DD}$ from Table I, at the 32nm process node the lower limit on efficiency F.O.M. from (9) is 1.3 fJ/step. This indicates an order-of-magnitude gap between the best reported F.O.M. in Figure 3 and the fundamental lower limit of the VCO-based architecture.

The result in (9) also indicates benefits of the VCO-based ADC approach:

- Scaling friendly: The ADC efficiency F.O.M. in (9) is the same as the energy per gate transition figure of merit in Table I, the reduction of which is the goal of digital scaling. Also, from (8) we see that achievable resolution in a given conversion time $T_{CONV}$ will improve as $t_{PD(MIN)}$ decreases at smaller geometry nodes.
- Reconfigurable resolution: From (8) we see that resolution can be increased simply by allowing more time $T_{CONV}$ for the conversion process. No reconfiguration of analog circuitry is required.
- Efficiency F.O.M. independent of resolution: From (9) we see that the efficiency figure-of-merit depends only on the supply voltage $V_{DD}$ and the gate load capacitance $C_L$. So if the ADC is reconfigured for a different point in the speed-resolution tradeoff space, the efficiency F.O.M. should be unchanged.

### *B. VCO jitter limited*

In general, the quantization noise portion of SNDR can be improved by increasing ADC resolution. The ability to trade an increase in conversion time for improved resolution without reconfiguring hardware is an advantage of this technique. As resolution increases, however, at some point noise performance will be limited by some fundamental aspect of the analog to digital conversion process. In this case, since we have moved A/D conversion into the time domain, a possible limit on ADC noise performance is oscillator jitter: the ability of the VCO to measure time accurately. In this section we drop the assumption of negligible VCO jitter; this can be considered a time domain approach complementary to the frequency domain approach of [15].

Figure 4 shows how jitter accumulates over a time interval $\Delta T$. Since the jitter in separate delay stages is caused by noise

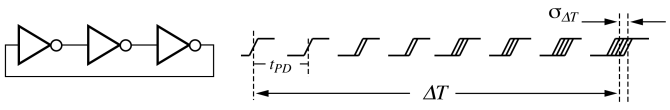


Fig. 4. Jitter accumulation in ring oscillator

in different MOS devices, we can assume the added noise in each stage to be independent, so the rms jitter increases proportional to the square root of delay [16], [17] and can be characterized by a figure of merit $\kappa$

$$\sigma_{\Delta T} = \kappa \sqrt{\Delta T} \tag{10}$$

For a VCO-based ADC, the time delay $\Delta T$ in (10) is the conversion time $T_{CONV}$.

The difficulty with noise occurs as we attempt to increase resolution $n_{MAX}$ by lengthening $T_{CONV}$ as indicated in (8). From (10) and Figure 4 we see that the rms jitter of the VCO will also keep increasing. To find the contribution of jitter to ADC noise as $T_{CONV}$ increases, we express the time error of (10) in ADC counts $\sigma_n$ by dividing by the gate delay $t_{PD}$

$$\sigma_n = \frac{\sigma_{\Delta T}}{t_{PD}} = \frac{\kappa \sqrt{T_{CONV}}}{t_{PD}} \tag{11}$$

For a worst-case analysis, the maximum noise occurs with the minimum $t_{PD}$ in (11); using (8) gives

$$\sigma_n = \frac{\kappa}{\sqrt{t_{PD(MIN)}}} \sqrt{n_{MAX}} \tag{12}$$

In [16], $\kappa$ for a full swing CMOS delay is approximated as:

$$\kappa = 2\sqrt{\frac{kT}{i_D V_{DD}}} \tag{13}$$

in which $k$ is Boltzmann's constant and $T$ is absolute temperature. Using (13) in (12) with (3) gives

$$\sigma_n = 2\sqrt{\frac{kT}{C_L V_{DD}^2}} \sqrt{n_{MAX}} \tag{14}$$

showing that the noise contribution due to jitter will increase as the square root of the target resolution $n_{MAX}$

To find the resolution at which the noise effect of jitter becomes appreciable, define $n^*_{MAX}$ as the resolution for which the rms noise due to jitter is just equal to the ADC quantization noise of $1/\sqrt{12}$ LSB:

$$\frac{1}{\sqrt{12}} = 2\sqrt{\frac{kT}{C_L V_{DD}^2}} \sqrt{n^*_{MAX}} \Rightarrow \boxed{n^*_{MAX} \approx \frac{C_L V_{DD}^2}{48kT}} \tag{15}$$

Evaluating (15) with $C_L$ and $V_{DD}$ from Table I gives $n^*_{MAX} \approx 6590$, suggesting that that jitter will limit noise performance for resolution above $\log_2(6590) = 12.7$ bits. The asymptote correponding to this limit is shown in Figure 3.

Further interpreting the result in (15) shows:

- The dimensionless quantity $n^*_{MAX}$ in (15) is the result of a ratio of two energies: the energy of the switching event $C_L V_{DD}^2$ relative to the random thermal energy $kT$. This makes intuitive sense since the noise effect of jitter will be of less concern as the random thermal energy is a small fraction of the switching energy which determines the time domain behavior of the delay stage.
- Referring to Table I, as switching energy per transition decreases with scaling, we expect the resolution $n^*_{MAX}$ to decrease, meaning that jitter will affect performance at lower ENOB.

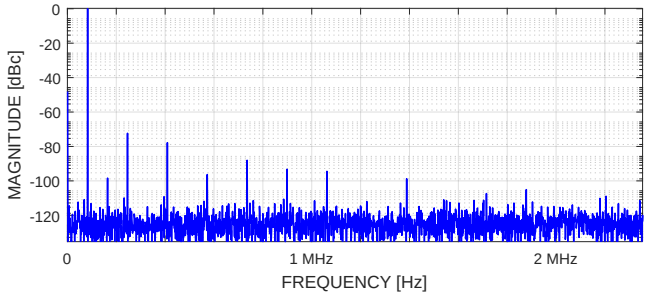


Fig. 5. VCO-based ADC output, frequency domain, ENOB 11.15b.

TABLE II
SIMULATION RESULTS SUMMARY

| Parameter | Configuration | | | Units |
|---|---|---|---|---|
| Resolution | 10 | 12 | 14 | bits |
| $f_S$ | 18.9 | 4.72 | 1.18 | MSps |
| ENOB | 9.47 | 11.15 | 12.46 | bits |
| Power (VCO only) | 22.8 | | | $\mu$W |
| F.O.M. | 1.70 | 2.13 | 3.43 | fJ/step |

- The limit in (15) was developed assuming a thermal noise jitter model. For channel lengths $< 100$nm, it is likely that $1/f$ effects [19]–[21] and/or excess noise [22], [23] will contribute additional noise beyond the prediction of (15).

## V. SIMULATION RESULTS

A VCO-based ring oscillator with background self calibration as described in [18] was simulated in a 45nm CMOS process. A 7-stage current-starved ring VCO as in Figure 2 was used, including the effects of VCO jitter in accordance with the model of (15). The ADC was reconfigured with different conversion times to target resolution of 10, 12, and 14 bits. Calibration was performed using MATLAB.

Figure 5 shows representative output in the frequency domain after calibration. Table II summarizes results for each of the reconfiguration cases, with ENOB and F.O.M. plotted in Figure 3. The F.O.M. results are in approximate agreement with the fundamental limit prediction of (9), and the F.O.M. for the reconfigured ADCs shows an increase with increasing resolution, as predicted by (15).

It should be emphasized that the results for [2]–[15] in Fig. 3 include the power contribution of additional circuitry for ADC linearization, whereas the F.O.M. for this work included only the VCO to more clearly show the fundamental limit. The gap in F.O.M. between [2]–[15] and the limit indicates the importance of implementing any additional circuitry necessary for ADC linearization with minimal additional power, thus preserving the inherent energy efficiency expressed in (9).

## VI. CONCLUSION

Analysis of a simplified model of the VCO-based ADC approach shows that there is an opportunity for order-of-magnitude improvement in efficiency F.O.M., with a quantization limit floor due to process energy per gate transition. Limitation due to oscillator jitter is expected to be appreciable only for ADC resolutions of order 12-13 bits, depending on process. Simulation results for a reconfigurable VCO-based ADC show conformance with theoretical predictions.

## ACKNOWLEDGMENT

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