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# Software Defined Radar

## Group 33 – Ranges and Test Beds

### MQP Final Presentation

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# Overview

- **Project Introduction & Deliverables**
- **Radar Background**
- **Radar System Design**
- **Time Synchronization**
- **Radar Processing**
- **Summary**

# Project Introduction

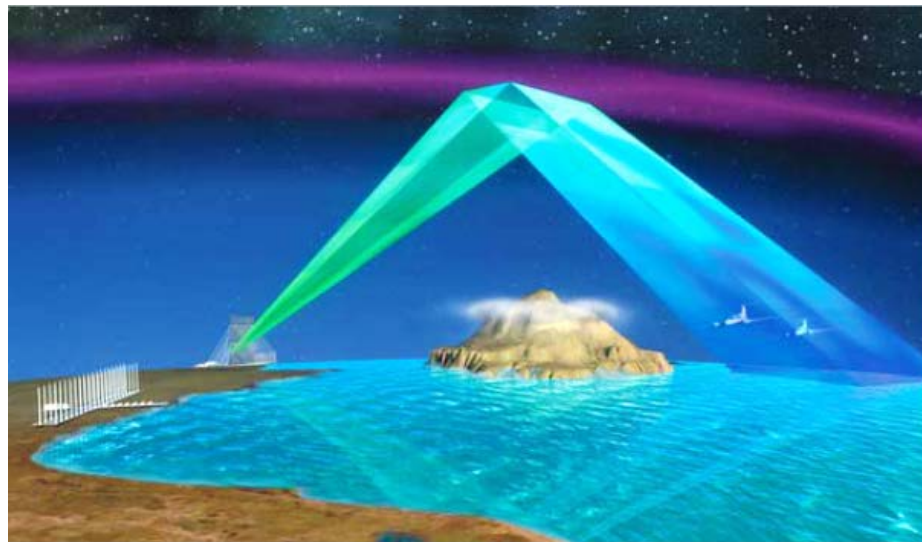
- **Project objective: build an inexpensive multistatic radar receive system using Ettus Universal Software Radio Peripheral (USRP2)**
- **Deliverables:**
  - **Time Synchronization**
  - **Radar Processing**
    - Range
    - Doppler
    - Direction
- **Software Defined Radio**
  - Radio whose typical hardware components are implemented in software
  - Digital filters & mixers, modulators/demodulators



<http://cwnlab.ece.okstate.edu/images/facilitiesimg/usrp2.jpg>

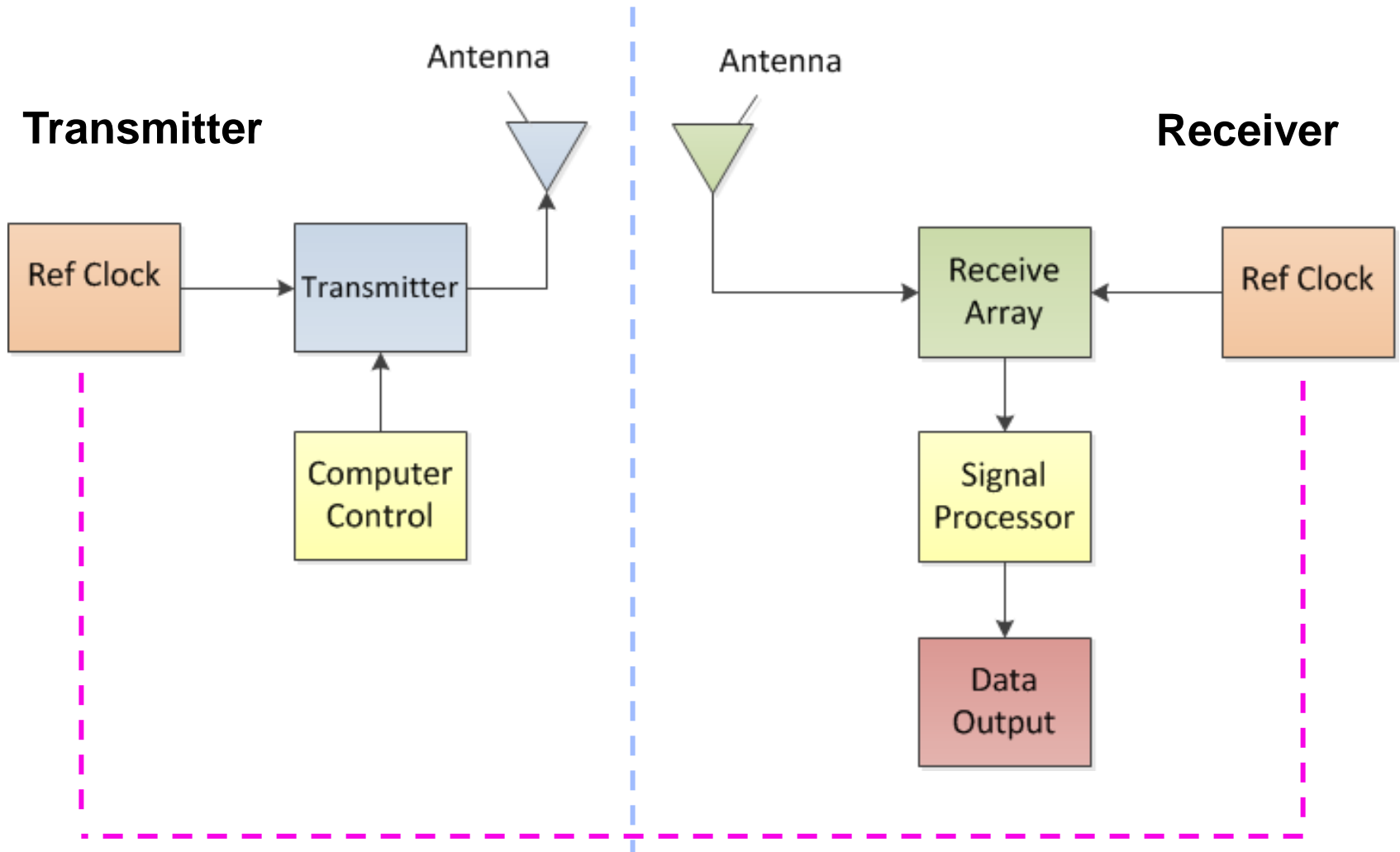
# Radar Background

- Radar, short for Radio Detection and Ranging, is a method of detecting targets using electromagnetic waves
- Two different types of Radar:
  - Pulse Radar
  - Continuous Wave Radar
- Over the Horizon Radar:
  - Continuous Wave
  - 3-30 MHz Frequency
  - Multistatic configuration
  - Large antenna arrays (~2-3 km)



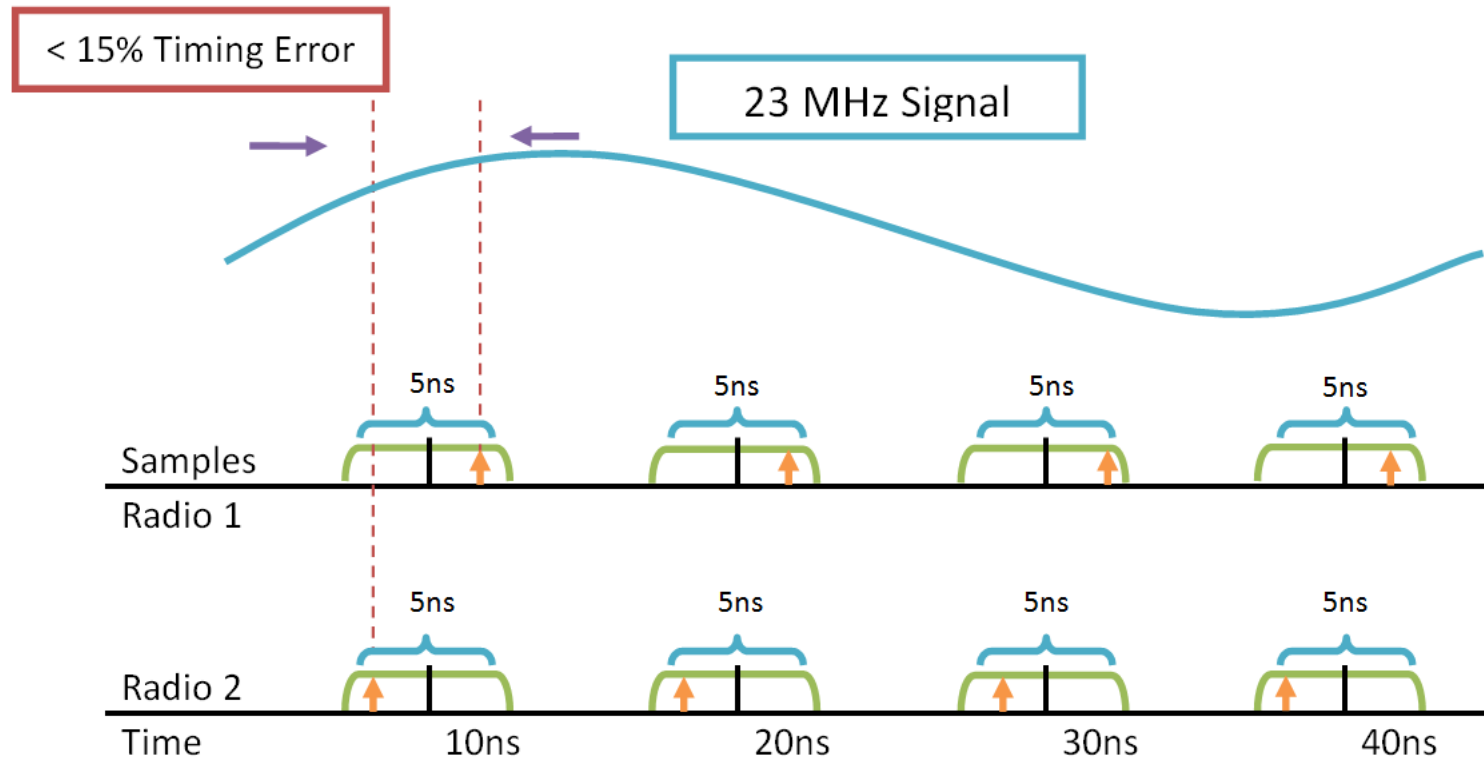
<sup>1</sup>[http://www.raytheon.com/capabilities/products/stellent/groups/public/documents/legacy\\_site/cms01\\_049201.pdf](http://www.raytheon.com/capabilities/products/stellent/groups/public/documents/legacy_site/cms01_049201.pdf)

# Multistatic Radar System



# Clock Synchronization

- **Sampling rate of the system is 100 MHz**
  - Our radar system operates in HF (3-30 MHz)
  - Tolerance of 5 ns minimizes the error to less than 15% for the HF band



# Clock Stability

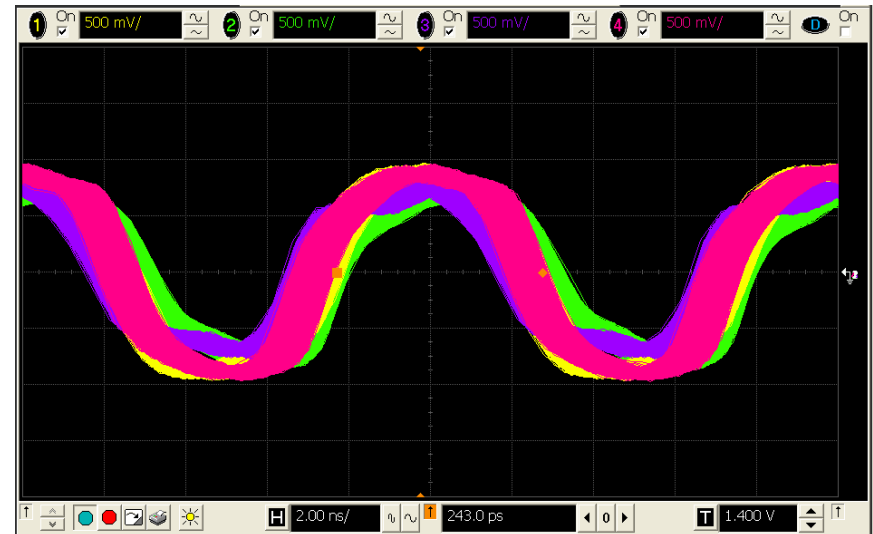
## Current Performance

3 Synchronized, 1 Not



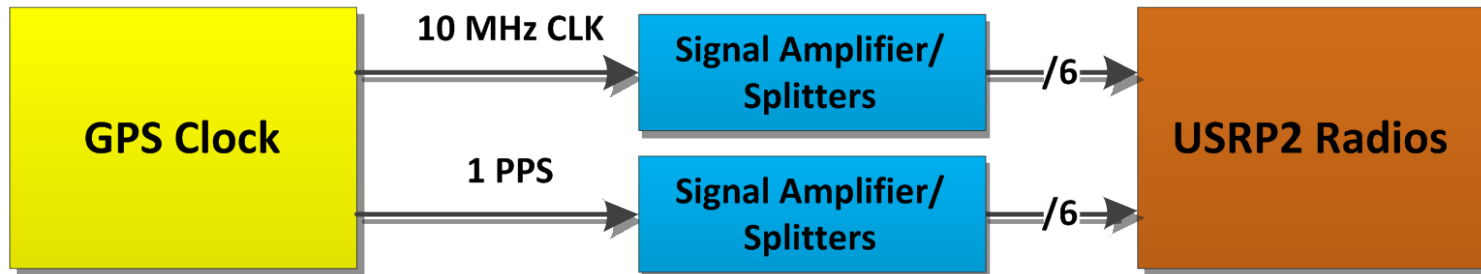
## Target Performance

4 Synchronized Radios



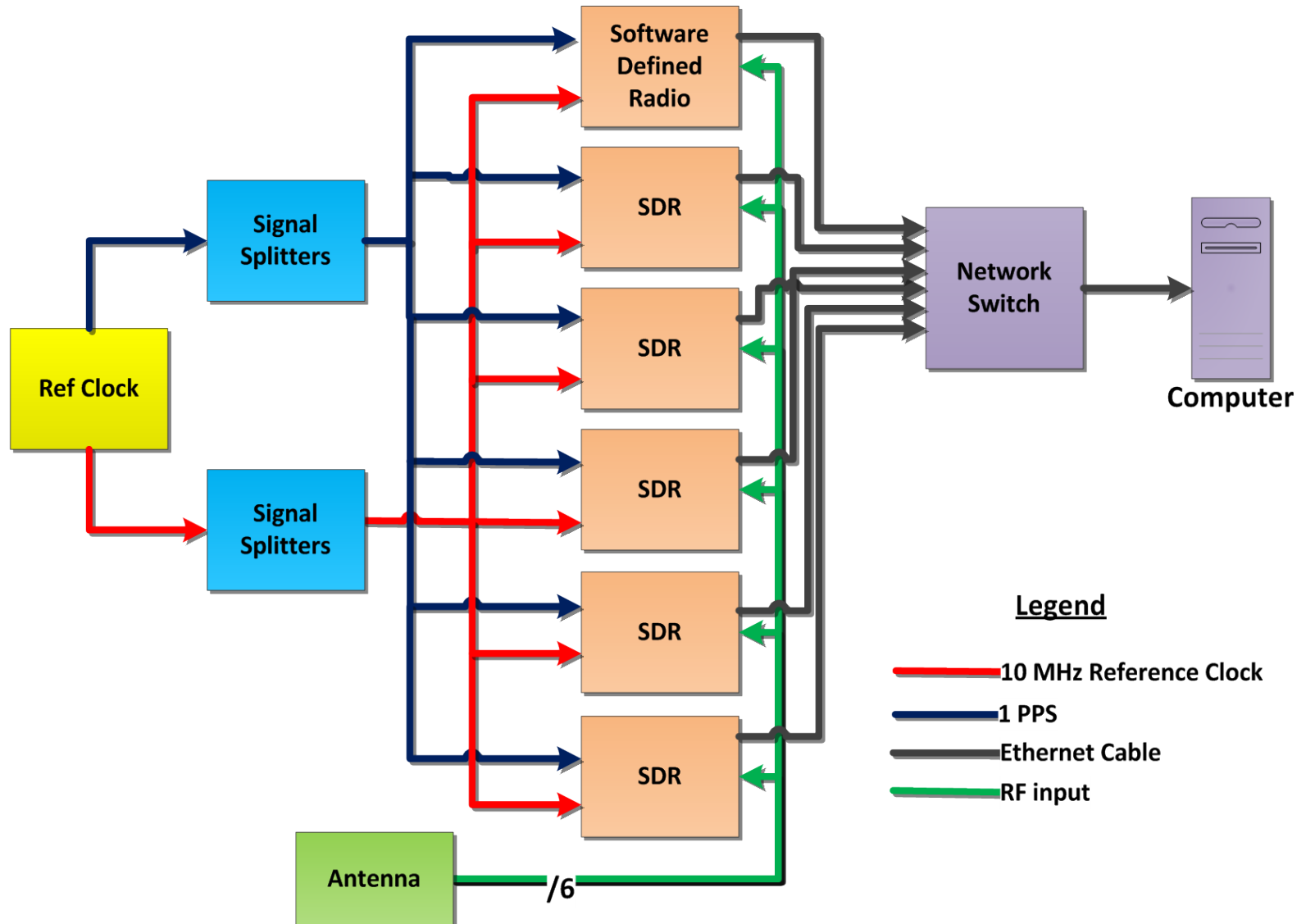
# USRP2 Clock Synchronization

- **Synchronizing USRP2 ADC Clock**
  - **100 MHz Internal Oscillator controlled by a Phased Locked Loop**
  - **Inputs to Phase Locked Loop**
    - 10 MHz Reference Clock**
    - 1 pulse per second (PPS )**
  - **Input Power/Level Requirements**
    - 10 MHz Ref. Clock Power: 5-15 dBm**
    - 1 PPS: 5V Peak-to-Peak**



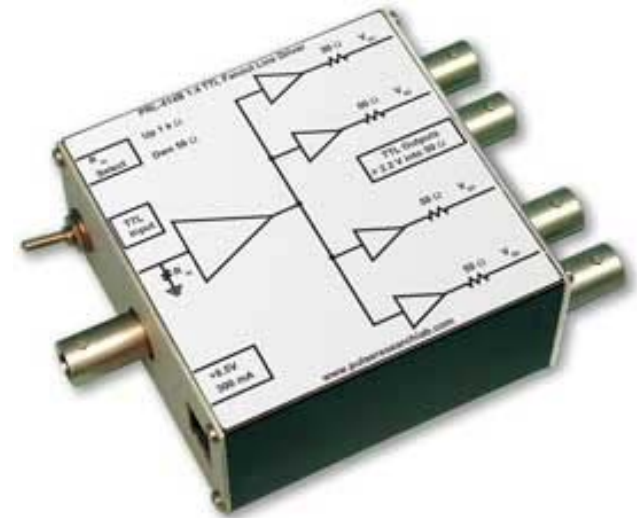


# Receiver System Design



# Radar System Design

- Selected the following Components:
- Jackson Labs GPS Disciplined Oscillator
  - 10 MHz output
  - 1 PPS output
- Pulse Research Labs 1:4 Fanout Buffer
  - Clock/PPS Signal Distribution
  - Freq < 100 MHz
  - Four in-phase 50Ω TTL Outputs

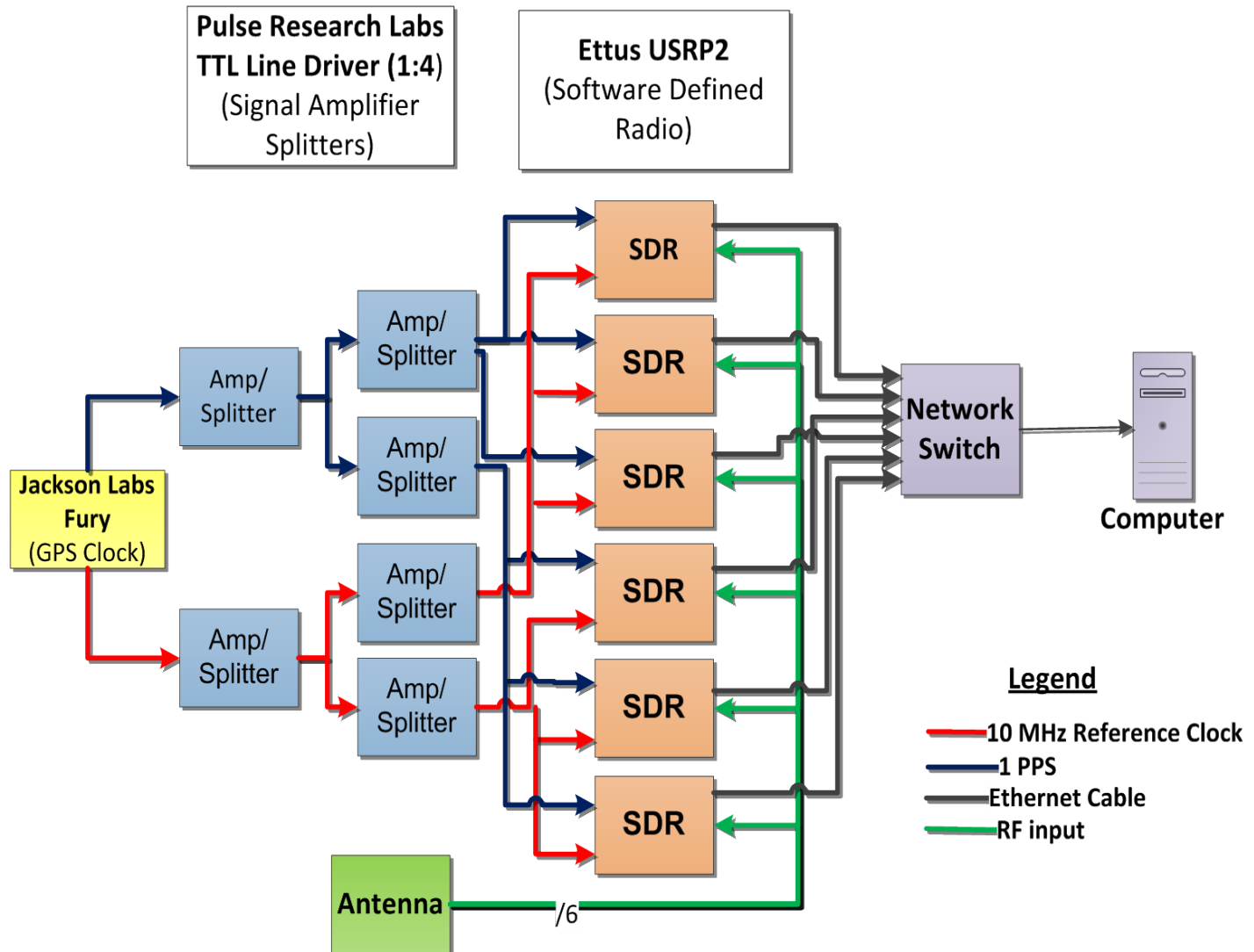


<sup>1</sup>[http://media.marketwire.com/attachments/200706/MOD-346700\\_Fury\\_bezeI\\_small.jpg](http://media.marketwire.com/attachments/200706/MOD-346700_Fury_bezeI_small.jpg)

<sup>2</sup>[http://www.pulseresearchlab.com/products/fanout/prl-414B/images/PRL-414B\\_small.jpg](http://www.pulseresearchlab.com/products/fanout/prl-414B/images/PRL-414B_small.jpg)

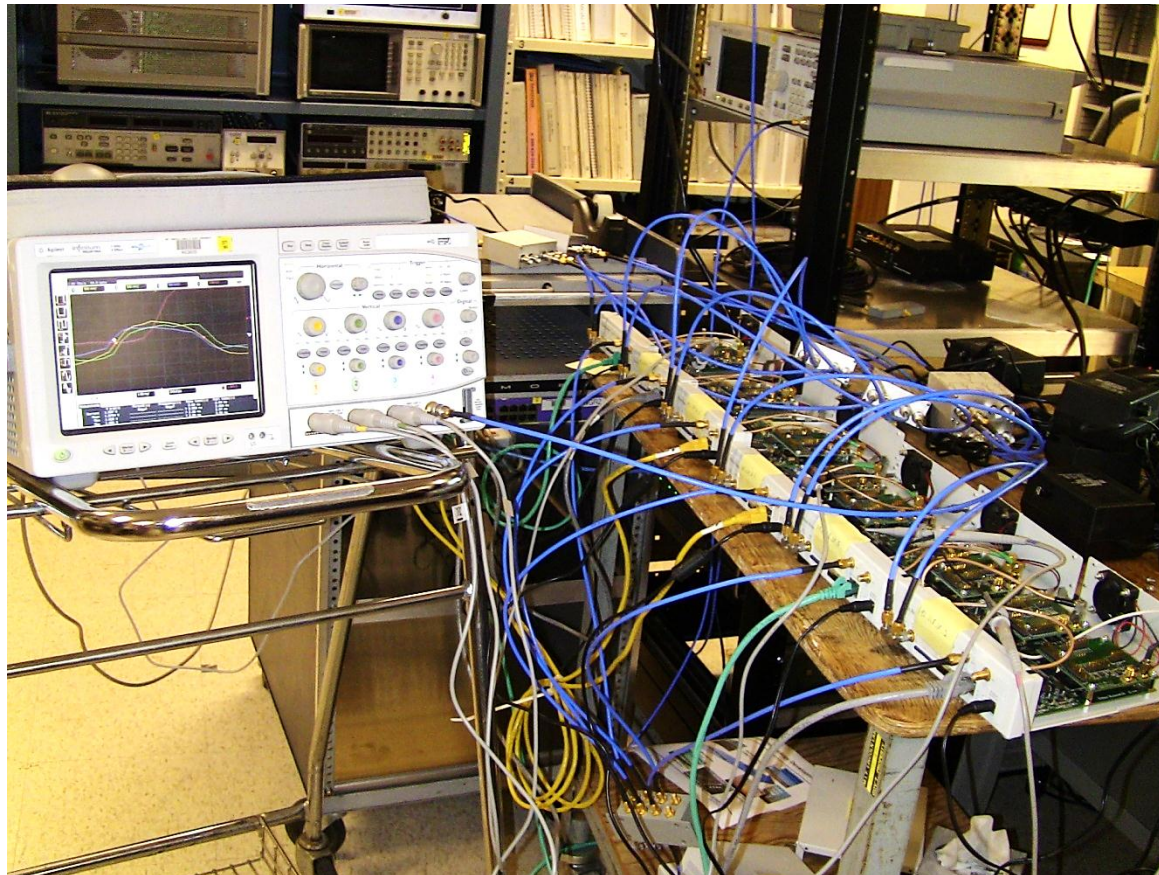


# Our Implementation



# Synchronization Testing

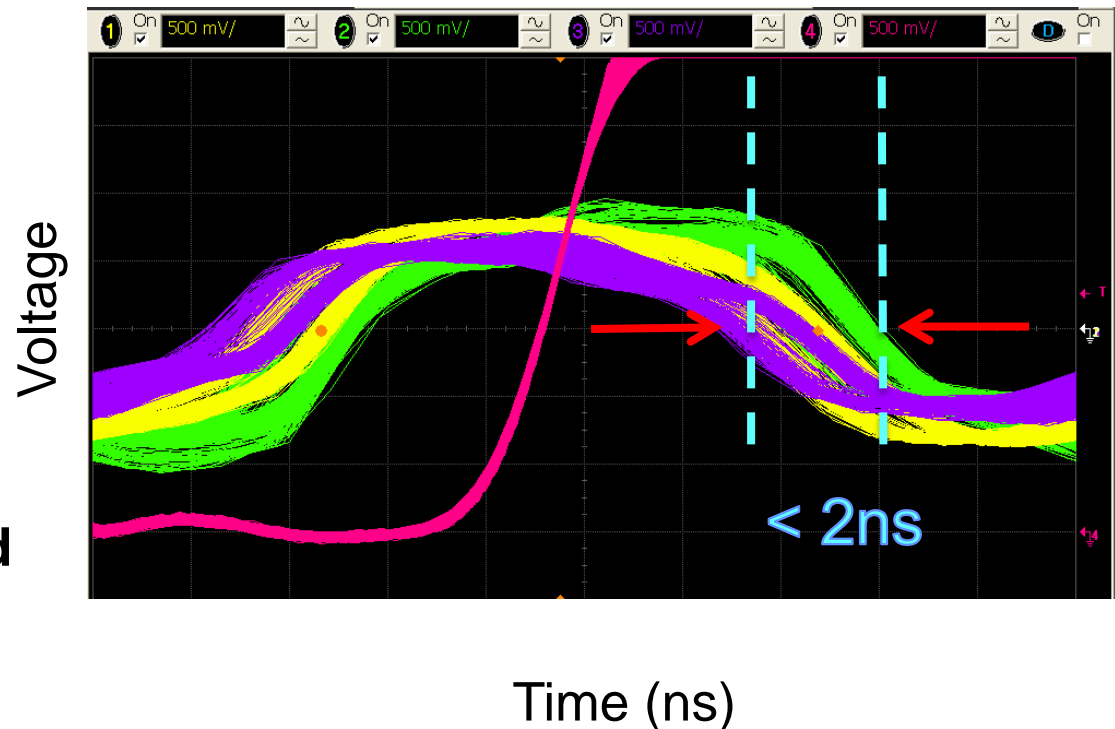
- We used an oscilloscope and the USRP2 clock debug pins to record the ADC clock drift



# PPS Trigger Test

- The purpose of this test was to determine whether the radios could consistently trigger off the 1 PPS
- Channels 1-3 were connected to USRP2s and Channel 4 was connected to the GPSDO PPS output
- The PPS signal served as a reference for measuring drift

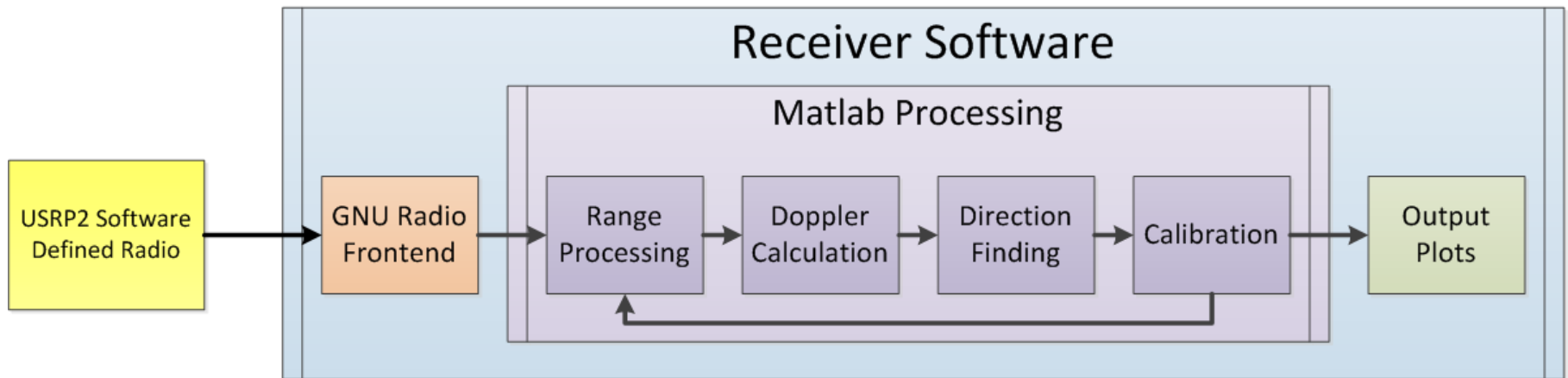
## 30 Minute Persistence Plot





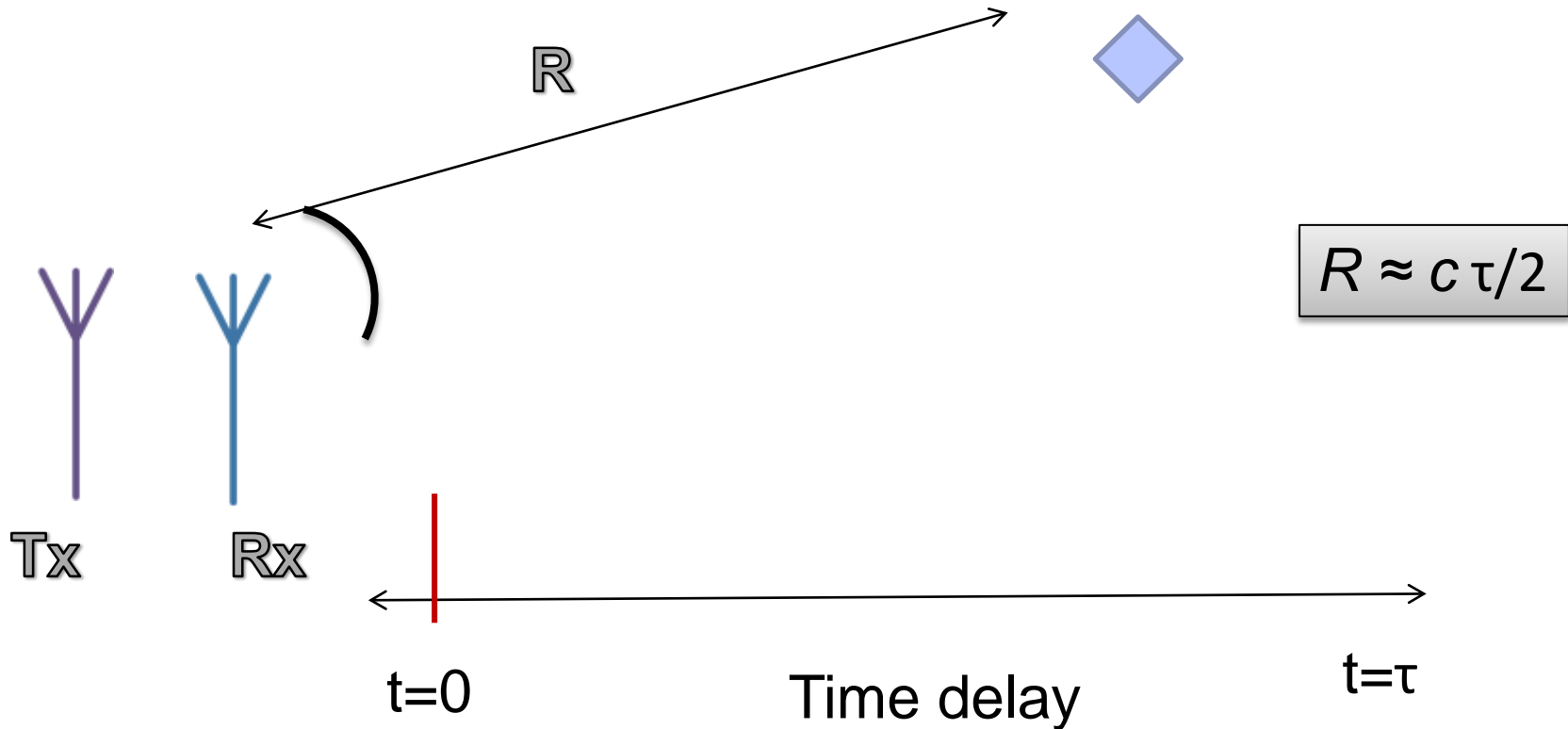
# Radar Receiver

- **GNU Radio provides the means to interface the USRP2 array and record data**
- **Radar processing implemented in Matlab**
  - Range
  - Doppler
  - Direction



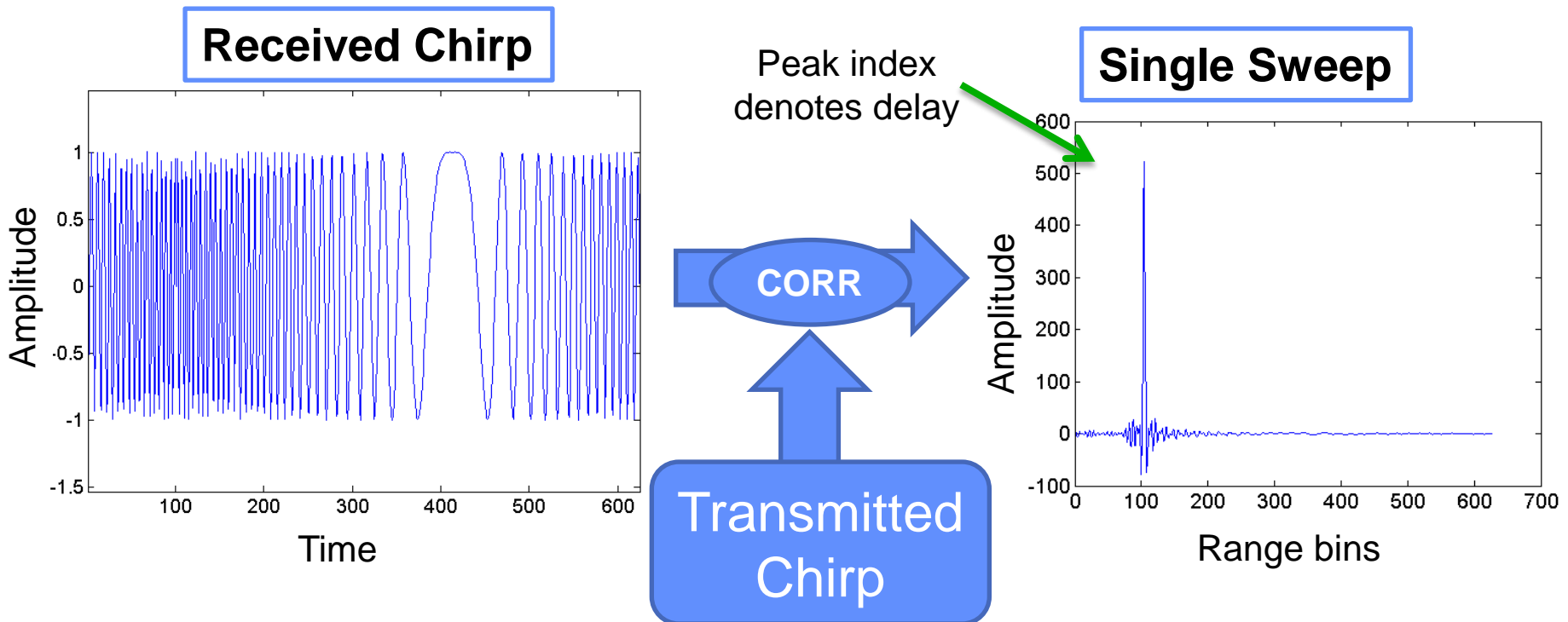
# Range Processing

- Range is determined by the time delay between the transmitted and the received signals
- Assuming the transmitter and receiver are synchronized, the delay equals the travel time



# Range Processing (cont.)

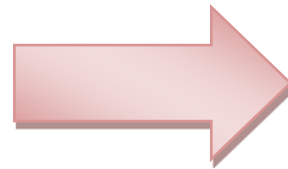
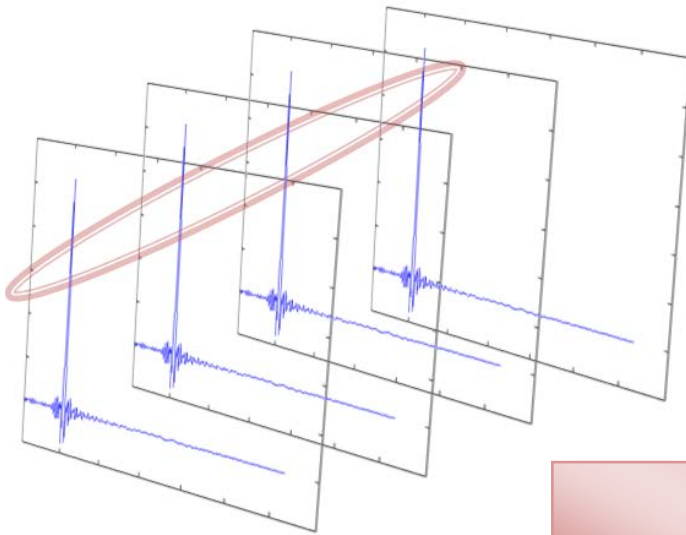
- The delay can be computed by determining when the chirp was received via correlation
- Correlating the received signal with the transmitted chirp is known as pulse compression



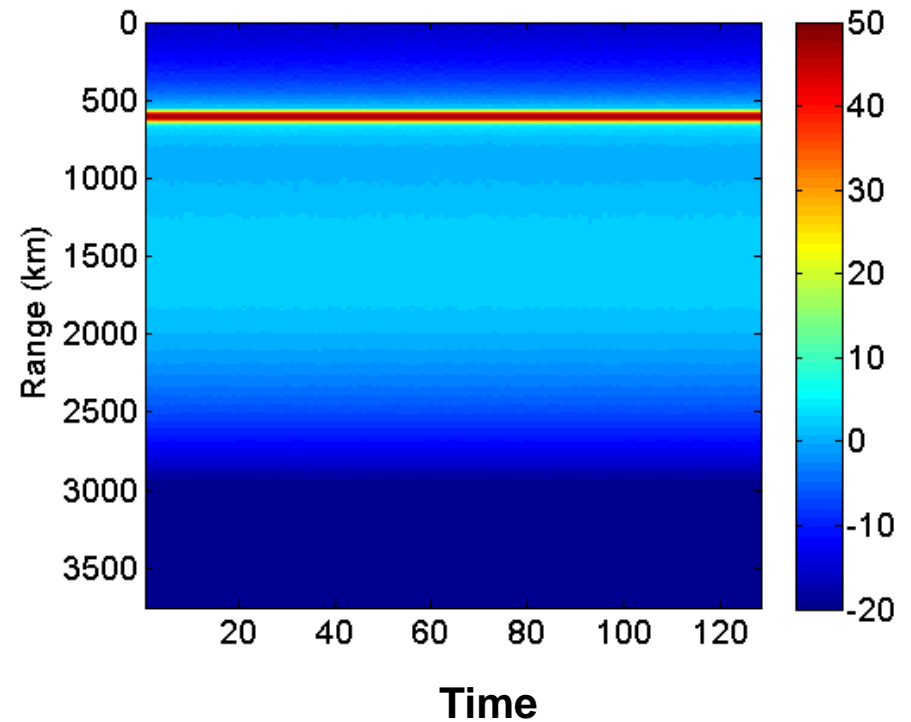


# Range Plot

Multiple sweeps  
over time



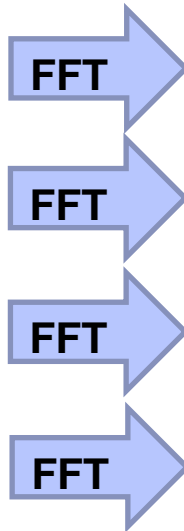
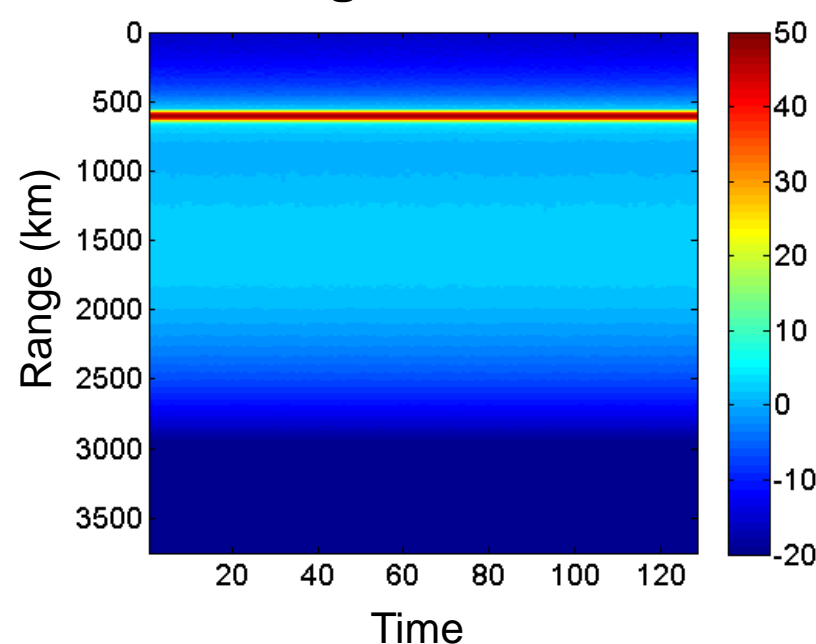
Range vs. Time



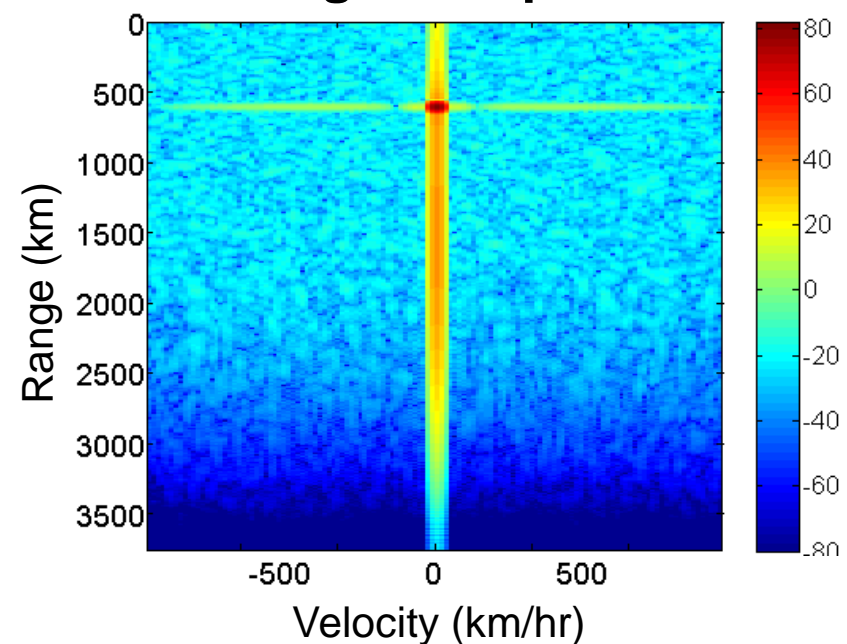
# Doppler Processing

- Used to identify target velocity
- Doppler is a phase progression from sweep to sweep
  - The Fourier Transform of a periodic function produces an impulse function at the center frequency
  - Taking the FFT of the range cells creates a peak at the intersection of the target's range and Doppler Frequency

## Range vs. Time

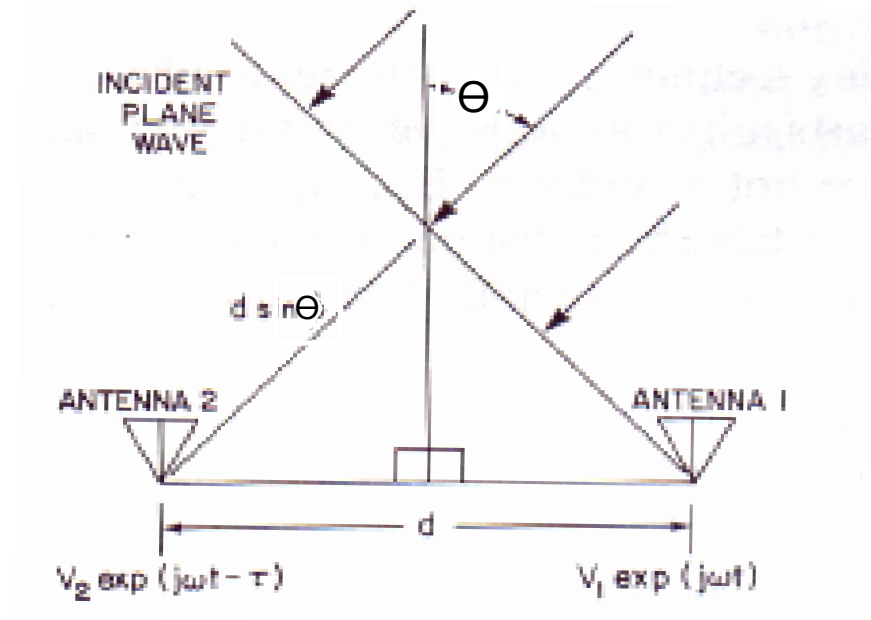
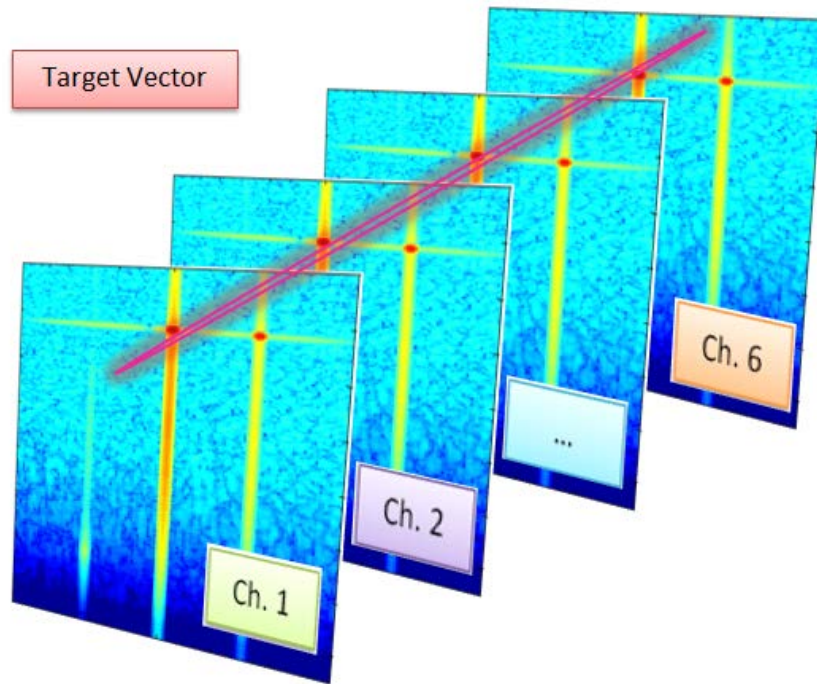


## Range vs. Speed



# Direction Finding

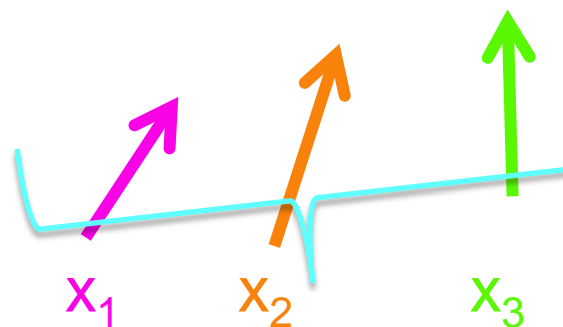
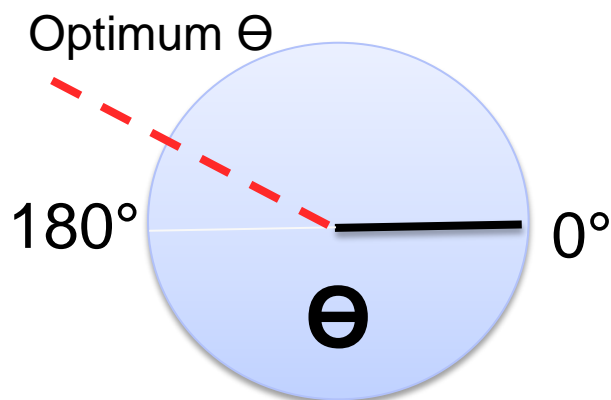
- Direction finding requires a vector of the complex samples from each channel's Range-Doppler plot
- Assuming a flat wave front (far field transmission), each sample has magnitude  $M$  and phase  $\Phi$ :  $M e^{j\Phi}$



$$\Phi(n) = \frac{2\pi}{\lambda} d(n - 1) \sin \theta, n = 1, 2, \dots, 6$$

# Direction Finding (cont.)

- Each point is multiplied by a candidate ‘zeroing vector’ defined for different theta values
- The value theta that optimizes the sum is the incident angle



Maximum  
magnitude sum

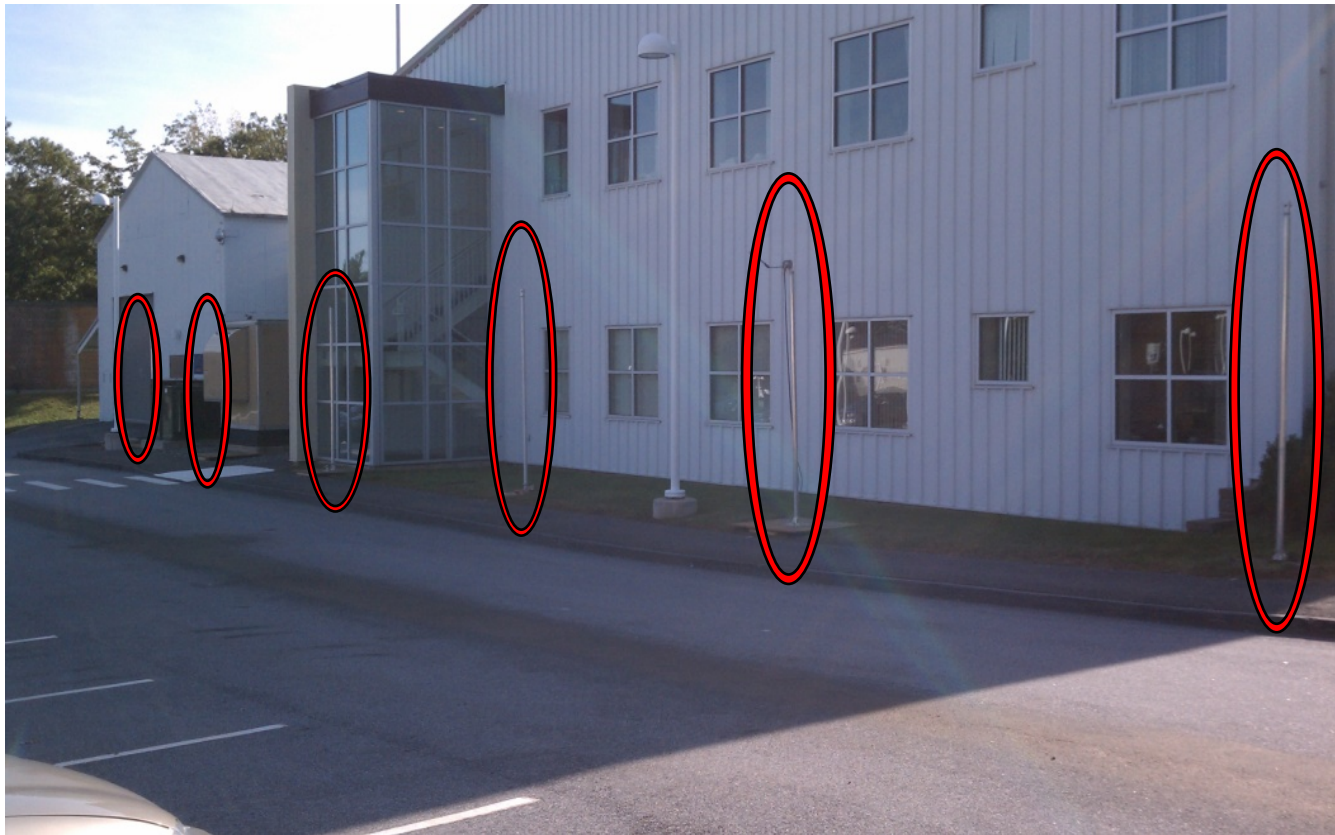
Complex samples  
from receivers at  
one Range-Doppler  
cell

$$\Phi(n) = \frac{2\pi}{\lambda} d(n-1) \sin \theta, n = 1, 2, \dots, 6$$

$$M e^{j\phi} * e^{-j\phi} = M$$

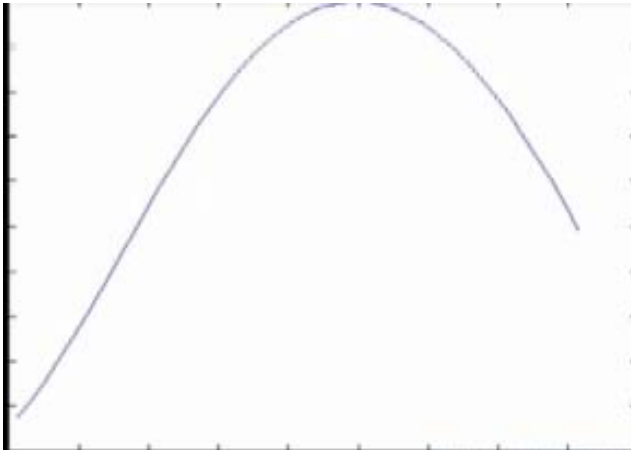
# Our Receive Array

- Six, 10 ft antennas arranged in a linear array outside Katahdin Hill





# Direction Finding Demonstration





# Summary

- **Purpose: Develop an inexpensive phased receive array using the USRP2 SDR**
- **Deliverables:**
  - Synchronized array
  - Array form factor
  - Radar processing code
- **Future Works**
  - Setup larger line array
  - Improve synchronization by modifying FPGA firmware
  - Implement Real-time Processing



# Acknowledgements

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# Questions?

