VCO-Based ADC With Digital Background Calibration in 65nm CMOS

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***Abstract*—This paper presents a mostly digital Voltage-Controlled-Oscillator(VCO)-based Analog-to-Digital Converter (ADC) with digital background calibration. "Split ADC" architecture containing two channels is utilized for the calibration technique. In each split ADC channel, two equivalent pseudo-differential VCOs are used to construct a differential system to alleviate the even order distortions, and a lookup-table based digital correction with 1st order interpolation is implemented in the ADC's backend for distortions and noise improvement. The proposed ADC combining VCOs and digital calibration engine simplifies the analog design procedure and takes advantage of scaling of CMOS to nanometer dimension. Simulation results in a 65 nm CMOS process targeting 13-b resolution achieves 12.5-b ENOB. DNL and INL are both within 1 LSB.**

I. Introduction

Nowadays, low-cost energy-efficient analog-to-digital converters(ADCs) are becoming more and more popular in a myriad of microelectronic application areas. In highly-scaled CMOS IC technology, dramatic improvement in digital power efficiency can be enabled, that drives many relevant ADCs research to focus on this attractive direction. Among these various ADC designs, voltage-controlled-oscillator(VCO)-based ADC is one favored candidate [1]- [8]. By taking VCO's inherent feature of phase accumulation, VCO can be used as an integrator in time-based ADCs. Usually, a phase measurement circuit is placed after VCO to convert the phase to digital numbers. However, because of the nonlinearity of VCO's voltage-to-frequency characteristics, instead of directly taking those digital numbers, additional procedures are needed to deal with the nonlinearity problem. Fig. 1 shows a typical v-to-f nonlinearity of VCO in 65 nm.

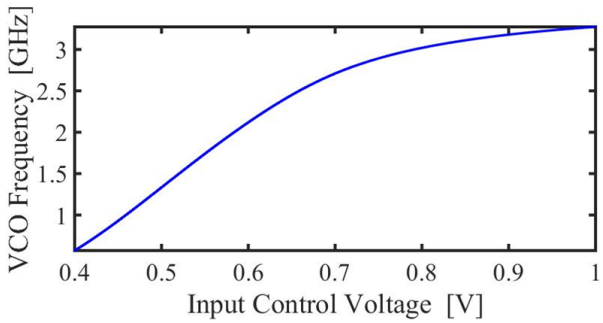

Fig. 1: Measured v-to-f characteristic of 11-stage ring VCO in 65 nm

There are lots of different kinds of approaches to improve VCO linearity. One prominent method that many papers have discussed is to implement VCO in $\Delta\Sigma$ architecture [1]-[4]. Inside the $\Delta\Sigma$ loop, the effects of VCO nonlinearity can be mitigated. However, this approach will also introduce extra digital-to-analog(DAC) or additional amplifiers, which consume more power and increase the complexity of the whole ADC design. Comparing with these $\Delta\Sigma$ ADCs, there still exist other accessible options by correcting nonlinear digital numbers in digital-domain directly without amending VCO's v-to-f nonlinearity in the analog circuit, which will remarkably simplify the VCO-based ADC's analog front end design in the future nanometer scaled CMOS technology.

This paper proposes a VCO-based ADC with digital background calibration in 65 nm CMOS process. A novel combination of simple analog frontend with digital calibration engine is discussed. First, section II present a brief overview of basic VCO-based ADC structure and its operating principles. Secondly, in section III, detailed design specifications of ADC's architecture including input ports, VCO types, phase collecting circuits, etc. are described. Thirdly, section IV presents digital background calibration, and how the calibration works appropriately with the frontend circuits. Simulation results of the 13-b resolution VCO-based ADC in 65 nm CMOS process and VCOs variations are displayed in section V. In the end, the conclusion of this paper is presented in Section VI.

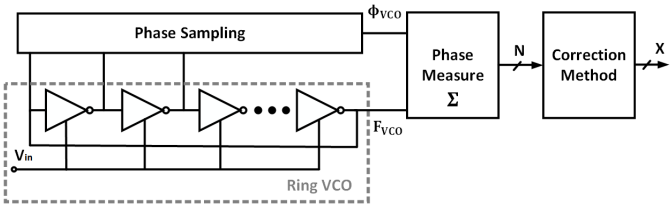

Fig. 2: A basic VCO-based ADC structure

II. VCO-based ADC Overview

The main principle of VCO-based ADC approach is to take advantage of the strengths of scaled CMOS process by transferring the analog signals to the time domain. In Fig. 2, a basic simplified VCO-based ADC in conceptual form is presented. The ADC input V_{in} is the control voltage of a ring oscillator. By changing the input voltage, the gate delay of inverters in the ring oscillator can be controlled; in other words, the

number of accumulated phase in one sampling period can be related with the input voltage, which transfers the voltage to the time-domain phase numbers. However, the output N of phase measurement circuit cannot usually be an ADC output. During the voltage-to-frequency transferring part, distortions are introduced because of VCO's v-to-f nonlinearity. Thus, additional procedures are needed to deal with the problem.

III. Circuit Architecture

The whole circuit is based on "split ADC" calibratable architecture [10] [9]. The primary idea of this ADC design is utilizing digital background calibration to correct the output codes from a coarse VCO-based ADC. The circuit can be divided into two parts for easier clarification:

1) Frontend: VCO core, sample and hold(S&H) input circuit and phase measurement circuit
2) Backend: all digital background calibration engine

This flexible two cascading stage circuit design gives a huge room to work with not only in VCO design part but also the digital calibration engine.

In Fig. 3, the schematic of frontend part is displayed. As to construct "split ADC" structure, there are two equivalent channels, A and B. Channel A is described in detail while channel B is omitted since it's exactly the same. Inside each channel, there are another two equivalent half circuits, called "positive" and "negative", which is named from their input voltage direction. The input voltages V_p and V_n are from same input source but in a 180-degree phase difference. Thus, any half circuits that are driven by V_n is called "negative half circuit", and similarly, any half circuits driven by V_p is called "positive half circuit".

A. Pseudo-differential VCO Constructed in Differential Mode

Ideally, an excellent VCO design providing high linear v-to-f characteristic can directly build a good performance VCO-based ADC. However, it usually introduces extra analog circuits. This design direction increasing analog circuit complexity is not suitable in the high-scaled CMOS technology. In this paper, as shown in Fig. 3 and Fig. 4, the VCO design is based on simple structure. Instead of concerning to design a high linear VCO, the whole systems linearity is focused by applying differential circuit structure.

To alleviate the v-to-f nonlinearity shown in Fig. 1, two equivalent half circuits are constructed. V_p and V_n are driving these two VCOs in a differential mode. For example, when V_p is rising from low to high voltage while V_n is falling from high to low (in 180-degree phase difference), the positive half circuit provides digital codes from small to large while the negative half circuit provides digital codes from large to small. Then, these two inverted digital codes are subtracted from each other to get a new differential digital output code. The equivalent system's v-to-f characteristic is highly improved since the differential structure removes the even order distortions and improves the noise performance.

The VCO is designed as a pseudo-differential ring oscillator which can provide gate delay's rising or falling time alternatively. Moreover, by utilizing the uniform quantization technique [4], the transition time to the phase decoder is uniformly spaced for any VCO frequency, which can mostly mitigate the nonlinear distortions.

The number of stages of VCO is carefully considered. Short odd number of stages like 5, 7 are not used, because the extreme high-speed VCO output cannot be collected correctly by the phase collecting circuit due to the technology time constraints. But a larger number of stages is also not recommended since it will waste area. Any non-prime odd number like 9 or 15 is not preferred since it sometimes induces overtone issues [13].

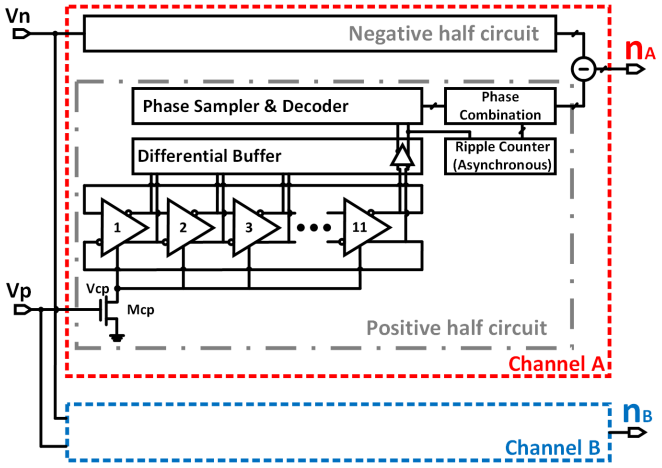

Fig. 3: Schematic of VCO and phase measurement circuit

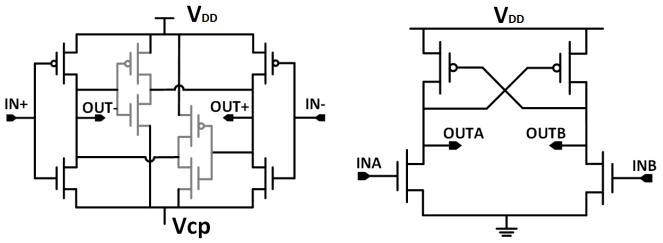

Fig. 4: Schematic of delay stage and buffer

B. Discrete Time Input Port: S&H Circuit

A bootstrapped sample and hold circuit is proposed [12]. It can not only provide a full scale of input swing but also give a quite reliable environment for adding dither technique which is required for digital background calibration.

C. Buffer and Phase Measurement Circuit Design

Directly connecting VCOs and phase measurement circuits may induce unpredictable problems. For instance, the driving ability of the output of VCO is too weak to drive the ripple counter, or sometimes VCO's output swing is smaller than digital threshold voltage. To avoid that, differential analog buffers are applied between them. It can certainly enhance the

driving strength of VCO output and stretch the small output swing to full scale. In Fig. 4, the schematic of differential buffer is presented.

Phase measurement circuits consist of phase sampler, phase decoder and ripple counter. To achieve higher resolutions, phase sampler and decoder are used to get decimal clock cycle(several phase delays make up a whole VCO clock cycle)

In one conversion period, phase sampler samples twice, at the beginning and the end respectively (to collect the difference of phase transferring in one conversion). Asynchronous counter (ripple counter) is used to count the clock cycles. The total number of transitioned phases N_{total_phase} can be expressed,

$$N_{total\_phase} = 2 * N_{stage} * C_{clock} + D_{phase\_difference} \quad (1)$$

where N_{stage} is number of VCO stages, C_{clock} is the counted number of VCO clock cycles, $D_{differential\_phase}$ is the phase code difference between start and end in one conversion period.

IV. Digtal Background Calibraion Engine

Based on "split ADC" calibratable architecture [10] [9], as presented in Fig. 3, the digital background calibration is operated as described in [8]. In addition to the available information in the references, the main differences and improvements of digital calibration in this application are explained.

Comparing with standard "split ADC", this novel differential version converts inputs V_p and V_n together with a half pseudorandom dither $\Delta V/2$,

$$V_{inA} = (V_p + p\frac{\Delta V}{2}) - (V_n - p\frac{\Delta V}{2}) = (V_p - V_n) + p\Delta V \quad (2a)$$

$$V_{inB} = (V_p - p\frac{\Delta V}{2}) - (V_n + p\frac{\Delta V}{2}) = (V_p - V_n) - p\Delta V \quad (2b)$$

where V_{inA} and V_{inB} are differential inputs of channel A and B respectively, p is pseudorandom number +1 or -1. The equivalent input voltage $(V_p - V_n)$, adding pseudorandom dither in such a differential way($\pm p\Delta V$), promotes the calibration engine performance in noise cancellation.

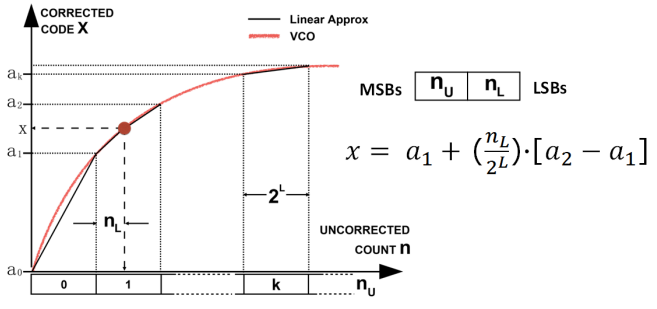

Fig. 5: Lookup-table-based 1st-order interpolation

The 1st-order interpolation based on lookup-table is displayed in Fig.5. The raw input n (digital codes directly from phase measurement circuits) is partitioned into MSBs part n_U and LSBs part n_L. The size of the upper MSB word, U bits long, determines the maximum number of points $M \leq 2^U$ in the lookup-table. For each value of the MSB word n_U , there is a corresponding corrected output code a_{n_U}. Within each segment, the value of the LSB word n_L is used to linearly interpolate between the adjacent a_{n_U} and a_{n_U+1} values in the lookup-table. Since the lookup-table points are separated by an amount 2^L on the n (uncorrected count) axis, linear interpolation gives the corrected output code x:

$$x_k = a_{n_U} + (\frac{n_L}{2^L})[a_{n_U+1} - a_{n_U}] \quad (3)$$

where x_k presents any corresponding corrected code, L is length of n_L.

After n_A and n_B are collected (shown in Fig. 3), these two raw counts go into the correction flow as shown in Fig. 5. With the lookup-table data cached in digital circuits, 1st-order interpolation is implement to get the corrected output code X_A and $X_A($ as demonstrated in equation (3)). And at the same time, the calibration algorithm is always working in the background. By using the Least-Mean-Square(LMS) feedback loop, the parameters in lookup-table are updated and nonlinear VCO v-to-f distortions are removed out after a certain calibration time. More algorithm details can be found in [8] [9].

V. Simulation Results

A. Calibration Performance

The proposed VCO-based ADC is designed and simulated in 65nm CMOS process. The calibration procedure was performed using MATLAB. The parameter and simulation results of the VCO-based ADC are shown in Table I.

Fig. 6 and Fig. 8 shows the DC linearity performance of the VCO-based ADC respectively. DNL remains in a similar range within -0.3/+0.3 LSB, and no missing code happens. Huge improvements are achieved for INL, it improves from -100/+100 LSB to -0.55/+0.48 LSB after calibration.

In Fig. 7, the frequency domain results are presented. Before calibration, due to the differential mode of VCOs arrangement, the even order distortions are almost canceled and the digital output code already has a relative good ENOB (6.97 b). Based on that, calibration engine mainly removes the 3rd, 5th, 7th and other odd order distortions, and ADC finally achieves an excellent ENOB (12.5 b). The calibration engine has the ability to improve the ENOB about 5-6 bit resolution. The estimated F.O.M (only VCO power) is relatively low and almost reaches VCO-based ADC's limits [11].

B. VCOs Variation Analysis

The variations of the four VCOs' v-to-f characteristics are also considered. To analyze the VCO variation effects to ADC's performance, additional variations of the v-to-f characteristic is applied to the VCO model. In Fig. 9, left up corner figure shows the v-to-f characteristic of VCO "A" and VCO "B" with 1% normal distributed deviation. Right

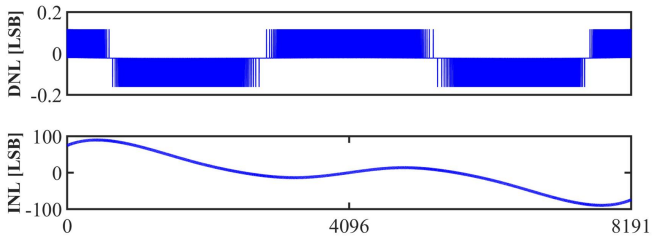

Fig. 6: DC linearity performance (Without calibration)

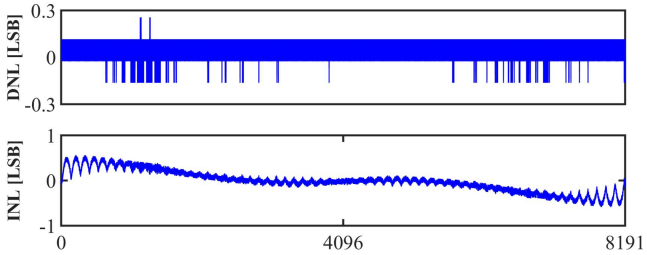

Fig. 8: DC linearity performance (With calibration)

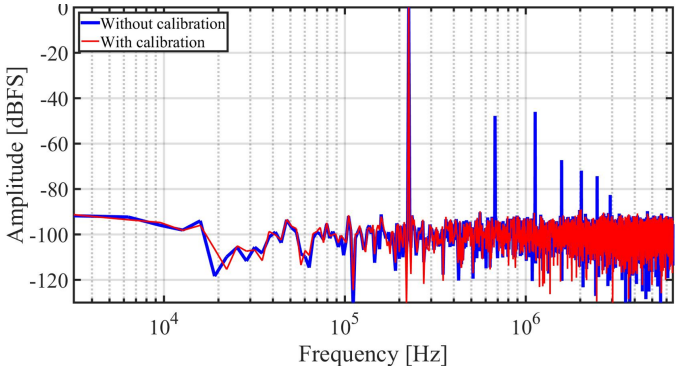

Fig. 7: Frequency domain results: 4096 points FFT

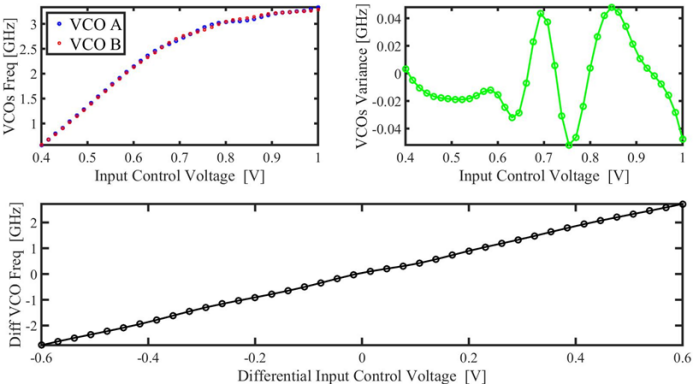

Fig. 9: VCOs v-to-f Variation Analysis

up corner shows the v-to-f differences of the VCO "A" and "B". With these deviations, the v-to-f characteristics of VCO "A" and "B" are severely ruined. However, the DC linearity of differential mode of VCO "A" and "B" is still good (DC linearity is about 6 bit) as presented in the bottom of Fig. 9. This indicates the variations of VCOs' v-to-f do not impact a lot to the differential VCO system. Furthermore, Monte Carlo simulation is also implemented. Fig. 10 displays 10,000 cases(VCOs with variations), whose DC linearity performance of differential VCO pairs is normally distributed (mean is 6.3 and variance is 0.08). As discussed the calibration engine has the ability of 5-6 bit improvement, the influence of different VCOs variation is not a significant problem.

TABLE I: PARAMETER / RESULTS SUMMARY

PARAMETER/RESULT		VALUE	UNITS
VCO	CMOS Technology	65	nm
	Fully Differential Input range	-0.6 - 0.6	V
	Sinlge VCO Frequency Range	0.57 - 3.27	GHz
	Sinlge VCO Power(with Buffer)	318	μW
ADC	Resolution	13	bits
	Sample Rate f_s	13	MSps
	Dither ΔV	3 %	FS
	DNL	-0.16 / +0.25	LSB
	INL	-0.55 / +0.48	LSB
	ENOB	12.5	bits
	Figure-of-Merit (FOM)	16.9	fJ/step
Calibration	Lookup-table Size	128	Points
	Calibration Time	0.08	sec

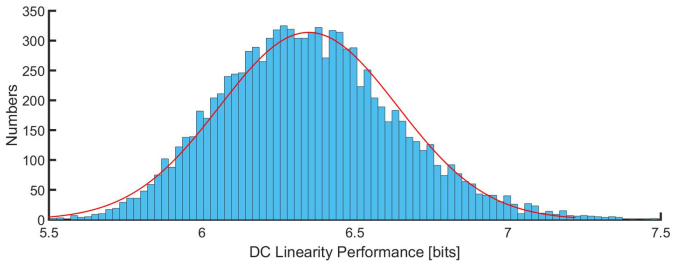

Fig. 10: DC Linearity Performance Distribution of Differential VCO pairs (Without Calibration)

VI. Conclusion

This paper has presented a mostly digital VCO-based ADC with digital background calibration. The ADC is constructed according to "split ADC" calibratable architecture, and its novel and straightforward design by combining differential arrangement of VCOs and digital calibration engine provide another applicable option for VCO-based ADC creation. Simulation results in a 65 nm CMOS process targeting 13-b resolution achieves 12.5-b ENOB, which confirm the performance of the proposed circuit architecture.

Acknowledgment

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